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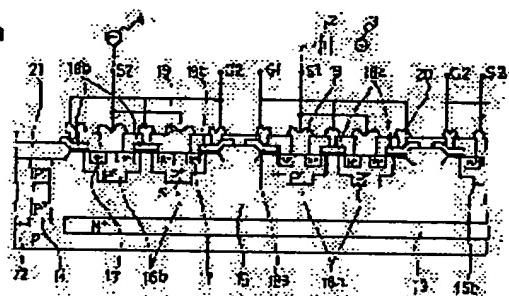
(21)Application number : 08-154246 (71)Applicant : SANYO ELECTRIC CO LTD
(22)Date of filing : 14.06.1996 (72)Inventor : OTAKE SEIJI

(54) SEMICONDUCTOR INTEGRATED CIRCUITS

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the loss of a circuit by integrating two MOSFET elements inside a common island region and making a common drain.

SOLUTION: An epitaxial layer 12 formed on a substrate is isolated to form an island region 15, and on the surface of the island region 15 P-type diffusion regions 16a, 16b, source regions 17, and gate electrodes 18a, 18b are formed. First and second MOSFET elements are formed by electrode wiring. By making the island region 15 a common drain, drain connection of the both is realized.



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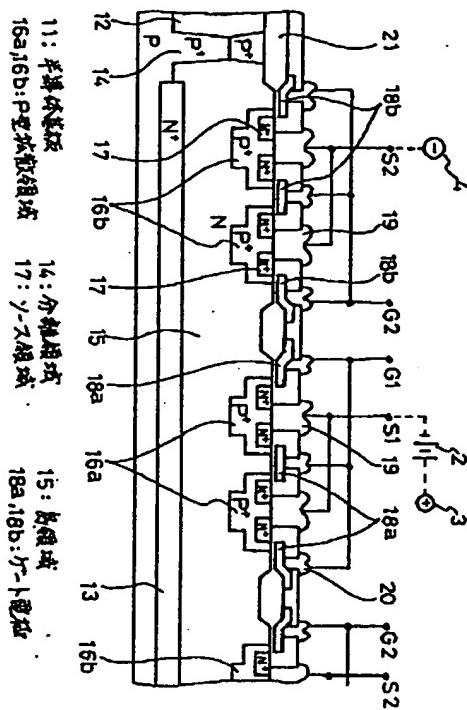
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(57) [要約] 2-DIMOSFET素子を共通の基盤面に形成する回路構成化した回路構成の低減効果。
 (解説) 基板上に形成した2-DIMOSFET素子を用いて、2-DIMOSFET素子を共通の基盤面に形成する回路構成の低減効果。
 第1回路構成15を共通K11とすると、K11の両端のK11-A
 第2回路構成16a、16b、Y-入力端子17、G1
 第3回路構成18a、18bを形成する。電極配線17、G1
 P型の抵抗構成16a、16b、Y-入力端子17、G1
 12を分離して基板上に形成する。基板面に
 12を分離して基板上に形成する。基板面に
 (解決手段) 基板上に形成した2-DIMOSFET素子を用いて、2-DIMOSFET素子を共通の基盤面に形成する回路構成の低減効果。

(54) [説明の各部] 半導体集積回路

(51) 申請番号	特開平8-154246
(22) 出願日	平成8年(1996)6月14日
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(43) 公開日	平成10年(1998)1月6日
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【特許請求の範囲】

【請求項1】 ドレインが互いに接続され、2次電池に直列に接続されると共に前記2次電池の充放電を制御する少なくとも2つのDSA(Double Diffused Self Alignment)型MOSトランジスタを具備する半導体装置であって、

一導電型の半導体基板の上に形成した逆導電型のエピタキシャル層を一導電型の分離領域により接合分離して島領域とし、

1つの前記島領域に、チャンネルとなる一導電型の拡散領域と逆導電型のソース領域及びゲート電極を形成して前記2つのDSA型MOSトランジスタを形成し、

前記2つのトランジスタの第1のゲートと第2のゲートの間に逆導電型の共通ドレン領域を設けて、前記2つのトランジスタのドレンを互いに接続したことを特徴とする半導体集積回路。

【請求項2】 前記DSA型MOSトランジスタが縦型のDSA型MOSFETであることを特徴とする請求項1記載の半導体集積回路。

【請求項3】 前記DSA型MOSトランジスタが横型のDSA型MOSFETであることを特徴とする請求項1記載の半導体集積回路。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】 本発明は、リチウムイオン、ニッケル水素などの充電可能な2次電池の充電回路に使われるDSA型のMOSFET素子を集積化した半導体集積回路に関する。

【0002】

【従来の技術】 リチウムイオン、ニッケル水素などの充電可能な2次電池は、ニッケルカドミウム電池に比べて容量を大きくできる反面、過電圧、過電流、過充電により電池性能が大幅に低下する欠点を合わせ持つ。そのため2次電池の端子間電圧を常時監視し、前記過充電等から前記2次電池を保護するための制御回路を具備する必要がある。そして、制御用のICと共に電圧駆動が可能なDSA(Double Diffused Self Alignment)型のパワーMOSFET素子を電池パック内に内蔵し、前記パワーMOSFETで2次電池の充放電流を制御することで電子機器の低消費電力化を図ることが多い。

【0003】 電池パック内に内蔵される回路の一例を図3に示す。図中、1は制御用のIC、2はリチウムイオン電池、3及び4は電池パック外部に導出される正極端子及び負極端子、5及び6は第1及び第2のMOSFET素子である。第1と第2のMOSFET素子5、6はドレンを共通接続しており、各々のゲートは制御用IC1の制御端子に接続されている。そして、前記過電圧、過電流、過充電時には制御ICからの制御信号を受けて第1と第2のMOSFET素子5、6の両方はどちらか一方がOFFする事により、リチウムイオン電池

2に流れる電流をカットして電池を保護するような動作を行う。

【0004】

【発明が解決しようとする課題】 図3の回路において、リチウムイオン電池2が放電動作を行う時、第1と第2のMOSFET素子5、6に図示矢印iのような動作電流を流すことになる。この時の抵抗成分Rは、MOSFET素子5、6のON抵抗や配線抵抗等により決まるものであるが、この値が大きいと前記動作電流により発熱し、該発熱は動作電流の損失となるので、2次電池の電池寿命を低下させることになる。そのため、抵抗成分Rを低下させることができれば電池寿命を延ばす鍵になっていた。

【0005】

【課題を解決するための手段】 本発明はかかる従来の課題に鑑みなされたもので、第1と第2のMOSFET素子を1チップ化したものであり、且つ、第1と第2のMOSFET素子を共通の島領域内部に形成し、島領域を共通ドレンとして互いのドレンを接続し、アルミ電極を省略することにより、抵抗成分を大幅に低減して電池寿命を改善できる半導体装置を提供するものである。

【0006】

【発明の実施の形態】 以下に本発明を図面を参照しながら詳細に説明する。図1は本発明による半導体集積回路を示す断面図、図2はその平面図である。まずは縦型のDSA型MOSFET(V-DMOS)を図示する。なお、図5中の符号と一致する箇所には同じ符号を付している。

【0007】 同図において、11はP型の単結晶シリコン半導体基板、12は基板11の上に気相成長して形成したN-型のエピタキシャル層、13は基板11とエピタキシャル層12との間に埋め込んで形成したN+型の埋め込み層、14はエピタキシャル層12を貫通してエピタキシャル層12を複数の島領域15に形成するP+型の分離領域、16a、16bは島領域15の表面に形成した複数のP型拡散領域、17はP型拡散領域16の表面に形成したN+型のソース領域、18a、18bはソース領域17近傍の上に形成したポリシリコンゲート電極、19はソース領域17とP型拡散領域16の両方にオーム接続するソース電極、20はアルミゲート電極、21はLOCOS酸化膜である。

【0008】 ゲート電極18aとP型拡散領域16aが第1のMOSFET素子5を構成し、同じくゲート電極18bとP型拡散領域16bが第2のMOSFET素子6を構成する。具体的には同じ島領域15内に単位MOSセルが多数個作られ、これらがアルミ電極により並列接続されて大きな2つのMOSFET素子5、6を構成する。隣接するP型拡散領域16a、16bの間にはLOCOS酸化膜が形成される。

【0009】 第1のMOSFET素子5のゲート電極18aはIC表面を引き回されて同じIC内部の別の箇所

に形成した制御回路の制御端子G1に接続される(図5参照)。同じく第1のMOSFET素子6のソース電極19はIC表面の外部接続パッドS1に接続され、電源パックとしては2次電池2の負極端子に接続される。2次電池2の負極端子は電源パックの正極端子3となる。【0010】第2のMOSFET素子6のゲート電極18bはIC表面を引き回されて同じIC内部の別の箇所に形成した制御回路の制御端子G2に接続される。同じく第2のMOSFET素子6のソース電極19はIC表面の外部接続パッドS2に接続され、電源パックの正極端子4となる。図2を参照して、ゲート電極18aとゲート電極18bとは櫛歯状に形成され、互いにかみ合うようにし配置することで、第1のMOSFETT素子5を構成するセルと第2のMOSFET素子6を構成するセルとが互い違いに隣接するように配置している。

【0011】第1のMOSFET素子5と、第2のMOSFET素子6は、一つの島領域15を共通ドレインとして一つの島領域15内に形成される。図4の回路図に従えば、両者のドレインは電気的に接続されなければよく、他に接続箇所がないので、島領域15表面にドレイン電極を導出する必要はない。本発明によれば、第1と第2のMOSFET素子5、6を集積化したことにより電流バスが短くなるのでドレイン接続に要する電気抵抗を減じることができる。さらに第1と第2のMOSFET素子5、6を共通の島領域15に形成したことにより、島領域15を共通ドレインにできるので、ドレイン接続のアルミ電極を不要として電流バスを短くでき、例えば両者を別々の島領域15に形成して電極接続する場合に比べてアルミ電極の引き回しが無い分、ドレイン接続に要する電気抵抗を大幅に減じることができる。

【0012】図3と図4はMOSFET素子として横型のDSA型MOSFET(L-DMOS)を形成した場

合の実施の形態を示す断面図と平面図である。同じ箇所には同じ符号を伏して説明を省略する。図1の縦型と異なりドレイン電流を基板11と水平方向に流すので、島領域15表面にドレイン領域22を具備する。P型拡散領域16a、ドレイン領域22、P型拡散領域16b、ドレイン領域22、P型拡散領域16a、と言うように交互に配置する。ドレイン領域22は電流バスの抵抗値を下げる働きをする。先の形態と同様にドレイン電極は不要ない。本実施の形態においても、島領域15を共通ドレインとすることにより電流バスを最短にできるので、ドレイン接続に要する電気抵抗を大幅に減じることができる。

【0013】

【発明の効果】以上に説明したとおり、本発明によれば、第1と第2のMOSFET素子5、6を共通の島領域15内に配置し、島領域15を共通ドレインとすることにより両者のドレインを接続したので、ドレイン接続に伴う電流経路の抵抗成分を大幅に減じることができ。従って図5の抵抗成分Rを大幅に減じることができるので、動作に伴う発熱を減じ損失を低減できるので2次電池の電池寿命を延長できる利点を有する。さらにドレイン電極を引き回す必要が無くなるので、アルミ配線を簡素化して面積の縮小を図ることができる。

【図面の簡単な説明】

【図1】本発明を説明するための断面図である。

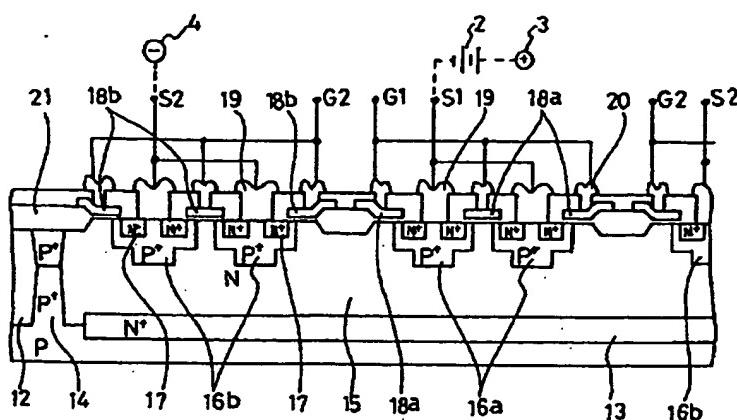
【図2】本発明を説明するための平面図である。

【図3】本発明の第2の実施の形態を説明するための断面図である。

【図4】本発明の第2の実施の形態を説明するための平面図である。

【図5】従来例を説明するための回路図である。

【図1】



11: 半導体基板

16a,16b:P型拡散領域

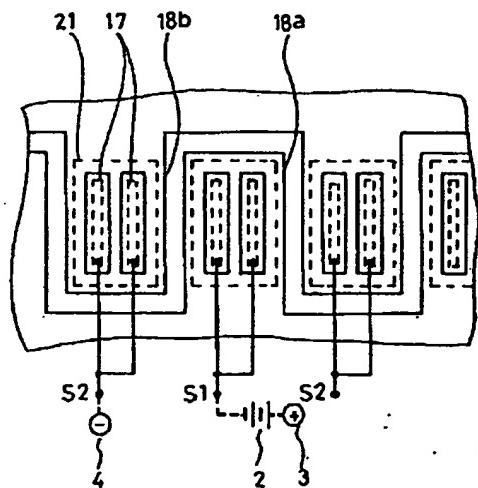
14: 分離領域

17: ヨース領域

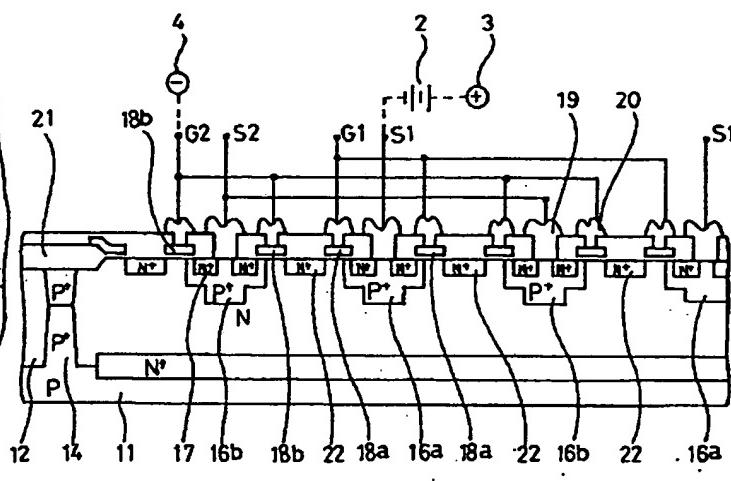
15: 島領域

18a,18b:ゲート電極

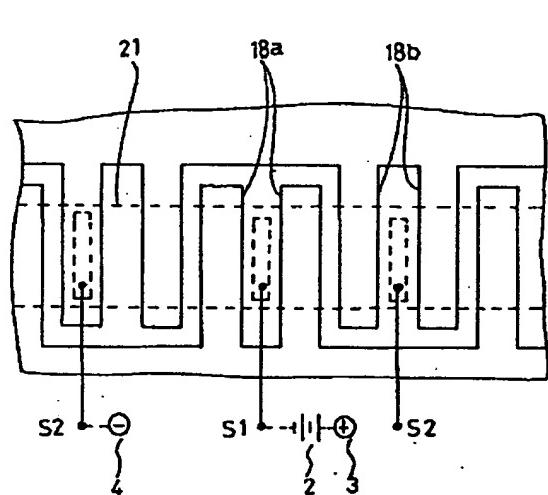
【図2】



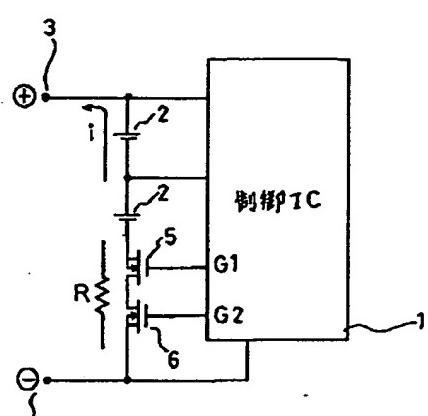
【図3】



【図4】



【図5】



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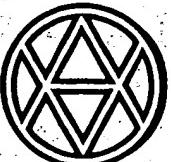
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1200V High-Side Lateral MOSFET in Junction-Isolated Power IC Technology Using Two Field-Reduction Layers

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Abstract

A lateral n-channel MOSFET structure in Junction-Isolated Power IC Technology using a P-type field-reduction region over a N-type field-reduction region for high-side and low-side switching applications is described. The concept of using two field-reduction layers have been verified by two-dimensional device simulations and by fabricating devices with breakdown voltage in excess of 1200V.

Introduction

In Power ICs in Junction-Isolated Technology, the control circuit consisting of low-voltage CMOS and bipolar devices can be easily integrated with a lateral power device when the substrate is at ground potential. For high-voltage lateral devices in Power ICs, a surface field-reduction region is widely used [1]. In lateral n-channel MOSFET structure with a single field-reduction layer (Fig. 1), the charge in the field-reduction region (N+) is such that it is completely depleted when the drain is at the line voltage and the source/body and substrate are at ground potential. This is useful for low-side switching applications.

Device Concept

The new device structure is shown in Fig. 2 for high-side configuration. Fig. 3 shows the device structure in this technology for low-side configuration. The device uses a P-type field-reduction layer over a N type field-reduction layer. The charge in the top (P+) field-reduction layer is chosen to be approximately $1 \times 10^{13} \text{ cm}^{-3}$ and the charge in the N- field-reduction layer is chosen to be from $1.5 \times 10^{12} \text{ cm}^{-3}$ to $2 \times 10^{12} \text{ cm}^{-3}$. This enables the use of the device as a high-side switch in Power ICs. In a high-side switching configuration, the drain is connected to the high line voltage.

There are many applications for power semiconductor switching devices which put the semiconductor device on the high-side. In those circuit applications, the semiconductor switch is connected between the high voltage line potential and the load. Consequently, both the source and drain electrodes of the power semiconductor switch will be placed at the high line potential while the substrate is at ground potential. If the conventional lateral MOSFET structure with a single field-reduction layer is used, the field-reduction layer would be completely depleted in this condition leading to PNP punch-through breakdown from the body region to the substrate. Consequently, Dielectric-Isolation Technology or discrete power MOSFETs with separate off-chip controls are used in high-side switching applications. The discrete device solution is costly in most applications. Dielectric-Isolation Technology has problem of heat-dissipation and is also costly.

In this paper, simulation and experimental results of a lateral n-channel MOSFET structure [2], which uses two field reduction layers is described. The charge in the N and P field-reduction layers and the field-reduction region length were varied in devices fabricated to look at influence of these parameters on breakdown voltage and on-state characteristics.

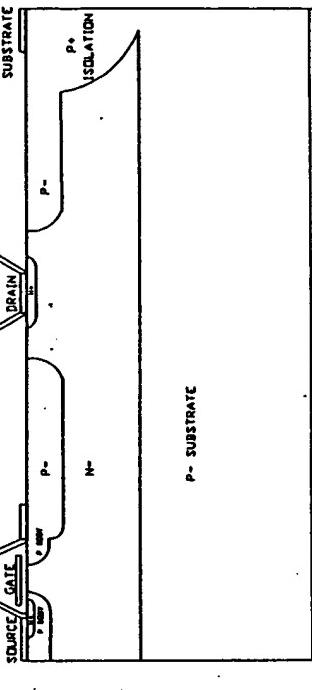


Fig. 2. Lateral n-channel MOSFET structure using two field-reduction layers for high-side switching applications

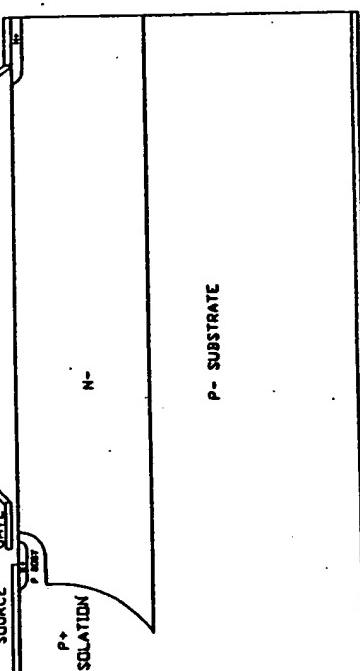


Fig. 1. Lateral n-channel MOSFET structure using a single field-reduction region

ISOLATION

SUBSTRATE

P+ SUBSTRATE

P+ ISOLATION

N+

N-

P-

SOURCE

GATE

DRAIN

ISOLATION

N+

P-

SUBSTRATE

P+ SUBSTRATE

P+ ISOLATION

N-

P-

SOURCE

GATE

DRAIN

ISOLATION

N+

N-

P-

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P-

SUBSTRATE

P+ SUBSTRATE

P+ ISOLATION

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Two-dimensional device simulations using PISCES-2B was used to get an insight into the device physics. The parameters used for device simulations are indicated in Table 1. The doping profile of the P₋ field-reduction region was obtained from SUPREM-3 process simulations.

Table 1. Parameters used for PISCES-2B two-dimensional device simulations

PARAMETER	VALUE
P- substrate doping (uniform)	$1.2 \times 10^{14} \text{ cm}^{-3}$
N- epi doping (uniform)	$1.2 \times 10^{15} \text{ cm}^{-3}$
N- epi thickness	20 μm
P- field-reduction region length	120 μm
Spacing between P- field-reduction layer & N+ drain diffusion windows	15 μm
Poly-silicon gate length of DRSPEN	8 μm
Gate oxide thickness	1000 \AA
Minority carrier lifetime	1 μs

A P₋ implant dose of $4 \times 10^{13} \text{ cm}^{-2}$ was used in the process simulation. The potential contours obtained from PISCES simulations are shown in Fig. 4 and Fig. 5 for the device off-state and on-state respectively. Fig. 6 and Fig. 7 shows the variation of potential through a vertical cross-section of the device at the center of the P₋ field-reduction region in the off-state and on-state respectively.

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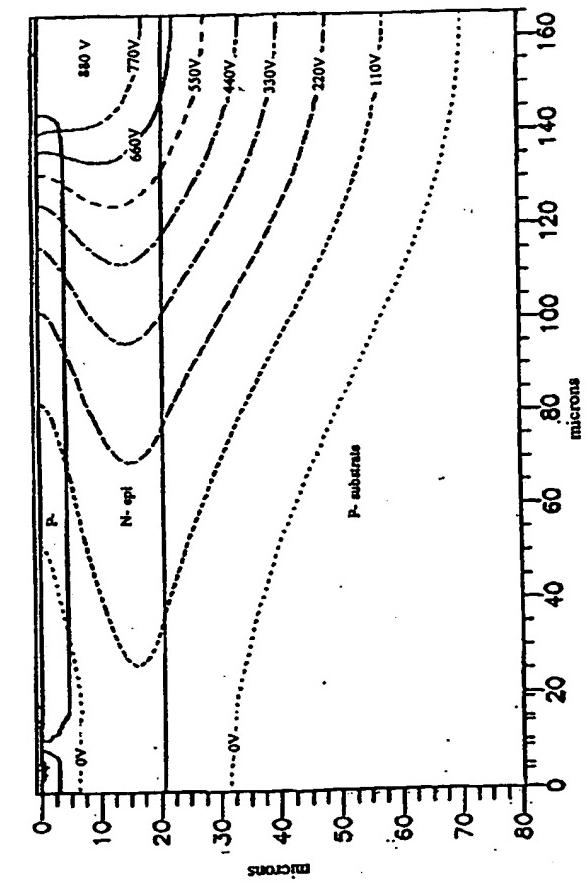


Fig. 4. Potential contours in the "two field-reduction layer" structure in the off-state (Drain at a high potential relative to the grounded source and substrate) from PISCES simulations

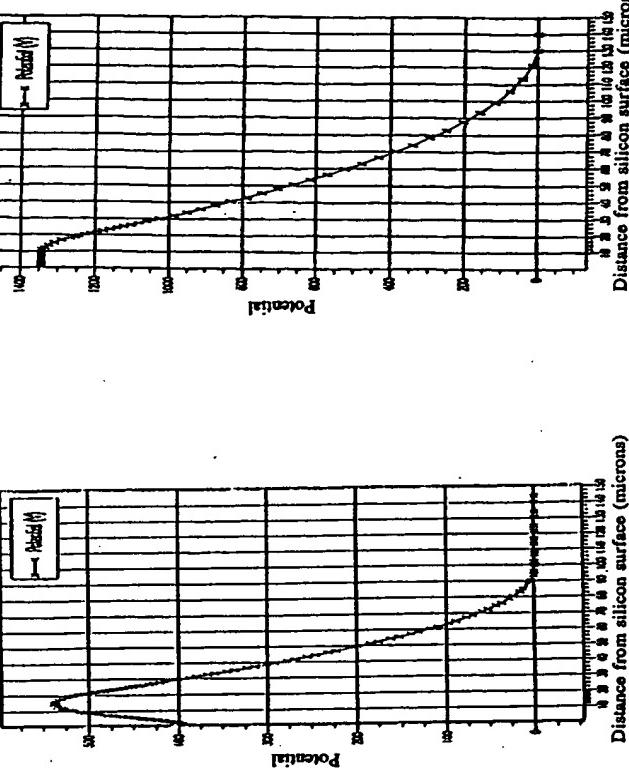


Fig. 5. Potential contours in the "two field-reduction layer" structure in the on-state (Drain and source at a high potential relative to the grounded source and substrate) from PISCES simulations

Fig. 6. Variation of potential through a vertical cross-section of the device at the center of the P₋ field-reduction region in the off-state from PISCES simulations

Distance from silicon surface (microns)

Distance from silicon surface (microns)

Fig. 7. Variation of potential through a vertical cross-section of the device at the center of the P₋ field-reduction region in the on-state from PISCES simulations

It can be seen from the potential distribution that in the off-state, the N- epi region is depleted from both the lower P+ regions under the N+ source and the upper P- field-reduction layer/N- epi region. The on-state potential distribution shows that in the on-state, the N- epi is depleted only from the bottom P- substrate/N- epi junction leaving sufficient undepleted charge in the N- epi to allow low on-resistance on-state current conduction. Breakdown voltages in excess of 1200V were obtained from simulation of the off-state and on-state of the device structure in the light-side configuration.

Device Fabrication

The device was fabricated using International Rectifier High-Voltage Junction-isolation (RV7) Power IC Process which is summarized below.

The starting material used is a N- epi of resistivity in the range of 4 Ω-cm on a P- silicon substrate of resistivity in the range of 100 Ω-cm. The first step in the process is the growth of an oxide of approximately 1 μm. The first mask is used to define the P+ isolation regions and is followed by a long drive in at high temperature. After this, the second mask is used to define the P- field-reduction region. The P- field-reduction regions are implanted with boron with a total dose in the range of $4 \times 10^{14} \text{ cm}^{-2}$.

Table 2. Experimental results for the first lot of devices fabricated. The breakdown voltage (BV) of the devices was measured at a drain current of 10 μA. The on-resistance ($R_{ds(on)}$) was measured at a gate voltage of 10V with respect to the source. The saturation current (I_{dsat}) was measured at a drain voltage of 10V with respect to the source.

SUBSTRATE RESISTIVITY (Ω-cm)	N- EPI RESISTIVITY (Ω-cm)	P- IMPLANT DOSE (cm ⁻²)	P- LENGTH = 100 μm	P- LENGTH = 120 μm			
				BV (V)	$R_{ds(on)}$ (Ω)	I_{dsat} (mA)	BV (V)
40	4.12	5.3×10^{13}	680	760	29	820	29
100	4.07	4.7×10^{13}	880	690	37	970	37
100	5.16	5.1×10^{13}	900	685	37	1100	740
100	5.3	4.1×10^{13}	890	710	35	1000	780
100	4.73	4.9×10^{13}	1020	600	44	1100	650
100	4.78	4.5×10^{13}	1100	600	44	1100	650
100	4.7	4.3×10^{13}	1020	590	45	1150	640

This is followed by the growth of a field-oxide of thickness approximately 1 μm. The third mask is used to define deep P+ regions under the N+ source regions of the MOSFET to increase its avalanche capability. The deep P+ regions are implanted with a boron dose of $4 \times 10^{14} \text{ cm}^{-2}$ after which drive in of deep P+ is carried out. The next mask is used to define the active regions of the devices in the Power IC. A gate oxide of 825 Å is then grown after which Polysilicon is deposited. Mask 5 is used to define the Polysilicon gate regions. The P body and N+ sourced/drain regions of MOSFETs are defined next. This is followed by the contact mask to define the contact windows. Metal is then deposited and defined using Mask 9. This is followed by deposition of passivation layer followed by definition of the pad regions using Mask 10.

Experimental Results

The experimental results for the device structure shown in Fig. 2 and in Fig. 8-9 for two lots of devices are summarized in Table 2 and in Fig. 8-9 for two lots fabricated. High breakdown voltage is obtained by choosing the right combination of P- field-reduction layer implant dose, N- epi resistivity, P- substrate resistivity, P- field-reduction layer length and P- field-reduction layer/N+ drain spacing.

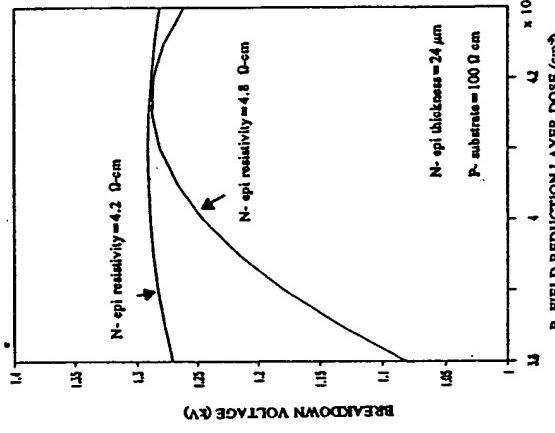


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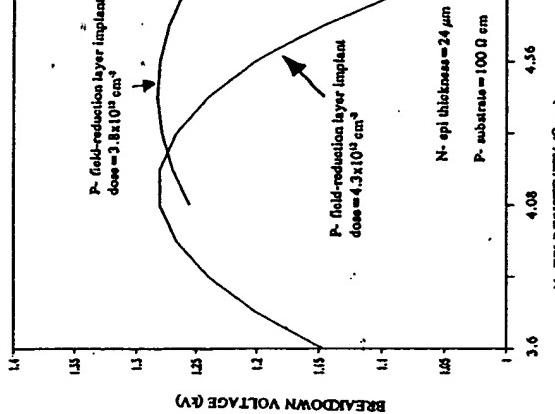


Fig. 8. Variation of breakdown voltage with P- field-reduction layer dose for the second lot of devices fabricated

Fig. 9. Variation of breakdown voltage with N- epi resistivity for the second lot of devices fabricated

In our process, breakdown voltage close to 1300V was obtained by using a P- field-reduction layer implant dose of $4.1 \times 10^{13} \text{ cm}^{-2}$, an N- epi resistivity of 4.2 Ω-cm and P- substrate resistivity of 100 Ω-cm. Another combination of parameters which resulted in breakdown voltage close to 1300V was a P- field-reduction layer implant dose of $3.8 \times 10^{13} \text{ cm}^{-2}$, an N- epi resistivity of 4.5 Ω-cm and a 100 Ω-cm P- substrate. The fabricated devices were of circular geometry with a P- field-reduction region length of 120 μm and had a on-resistance in the range of 900 Ω. The saturation current was in the range of 20 mA at a gate-to-source voltage of 10V. The devices were designed with a spacing of 15 μm between the P- field-reduction layer diffusion window and the N+ drain diffusion window.

Conclusions
The concept of using two field-reduction layers has been verified by two-dimensional device simulations and fabricating devices with breakdown voltage in excess of 1200V using Junction-Isolated Power IC process. The concept is useful for lateral devices in high-side and low-side switching applications.

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Self-shielding: New High-Voltage Inter-Connection Technique for HVICs

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Abstract

A new, cost-effective, high-voltage inter-connection technique for HVICs, named SELF-SHIELDING, is proposed. To avoid the lowering of breakdown voltage of high-voltage devices affected by the electric potential of overlying inter-connections, self-shielding technique utilizes only the native PN-junction structures of high-voltage devices themselves. No additional shielding structure is required even to realize a very high-voltage IC above 1000V. Design concept and device structures are presented together with the experimental results on the operation of self-shielded 1200V level-shifters.

Introduction

The most critical theme for high-voltage integrated circuits (HVICs) is the electrical shielding of inter-connections from underlying high-voltage devices. If the inter-connections lying over high-voltage devices in HVIC are not properly shielded, the electric potential of inter-connections affect on the electric field distribution of underlying high-voltage devices. As a result, the breakdown voltage of the high-voltage devices are severely lowered.

To avoid this lowering of breakdown voltage, several approaches have been reported. Fixed potential shielding plates were successfully applied to 300-400V class HVICs [1,2]. Capacitively coupled field plates [3,4] and resistive field plate [5] obtained good results in 500-600V class HVICs. However, the extension of these techniques to higher voltage requires proportional increase of insulator thickness and additional conductive layers, to be resulted in the increase of cost and process difficulties. It was these limitations that prevented the development of HVIC far below 1000V.

In this paper, to breakthrough above mentioned limitations in conventional approaches, we propose a new shielding technique of high-voltage inter-connections for very high-voltage ICs; named SELF-SHIELDING [6]. After describing conventional HVIC, we demonstrate the design concept and device structures of self-shielded HVIC, followed by the experimental results on the operation of self-shielded, 1200V, n- and p-channel level-shifters.

Conventional HVIC

Typical block diagram and floor plan of conventional HVIC for driving totem-poled insulated-gate bipolar transistors (IGBTs) are shown in Fig. 1 (a) and Fig. 2 (a), respectively. GDUH and GDUL in Fig. 1 are the driving circuits, respectively, for high- and low-side IGBTs. They are supplied driving power by low-voltage supplies (Vcc) connected to N terminal for GDUL and to O terminal for GDUH. Control unit in Fig. 1 is supplied by the same Vcc as GDUL and generates the timings for driving IGBTs, for example, to control a motor connected to O terminal. High-voltage main supply (Vdd) is connected between P and N terminals. As the potential of O terminal (Vo) swings between the potentials of P and N terminals (Vp and Vn) along with the switching of IGBTs, GDUH (Vo-level circuits) are isolated from GDUL and control unit (Vn-level circuits). To ensure this isolation, PN-junction-isolation and high-voltage junction termination (HVJT) techniques are used. For transmitting signals between Vo- and Vn-level circuits, level-shifters are provided utilizing high-voltage, n- and p-channel MOSFETs (HVN and HVP), load resistors, and voltage-clamping diodes.

In this design of conventional HVIC, high-voltage inter-connections (HV inter-connect.), H1 and H2, are crossing over HVJT respectively at two portions. At these portions, electric shielding is required to avoid the breakdown voltage lowering of HVJT affected by the electric potential of HV inter-connections. Conventional shielding techniques forced HVICs into increasing cost and process difficulties [1-5]. What is worse still, those process difficulties, mentioned earlier, limit the maximum breakdown voltage of conventional HVICs below 1000V.

Design Concept of Self-Shielding

In self-shielding concept, HV inter-connections do not cross over HVJT. Therefore, the electric potential of HV inter-connections are automatically shielded by self-junction structures of high-voltage devices.

Block diagram and floor plan of self-shielded HVIC are shown in Fig. 1 (b) and Fig. 2 (b), respectively. As seen from these figures, three loops of HVJT in conventional HVIC for

p-substrate and the drain of HVP. The parasitic resistance causes undesirable leakage current parallel to the road resistors of level-shifters. As the parasitic resistance is unavoidable in proposed structures, it must be controlled to substantially high value for suppressing the power dissipation of self-shielded level-shifters.

Experimental Results

Experimental run has been performed to evaluate the applicability of self-shielding technique to very high-voltage ICs over 1000V. Substrates used were $230\Omega\text{cm}$, boron-doped, floating-zone-melted, silicon wafers and the process used was 3 μm -CMOS. Evaluated devices were HVN, HVP, self-shielded HV n- and p-channel level-shifters, and the parasitic resistors of self-shielding regions. N- and p-channel level-shifters were laid into a single, complementary device. The photograph of a pair of complementary level-shifters is shown in Fig. 4.

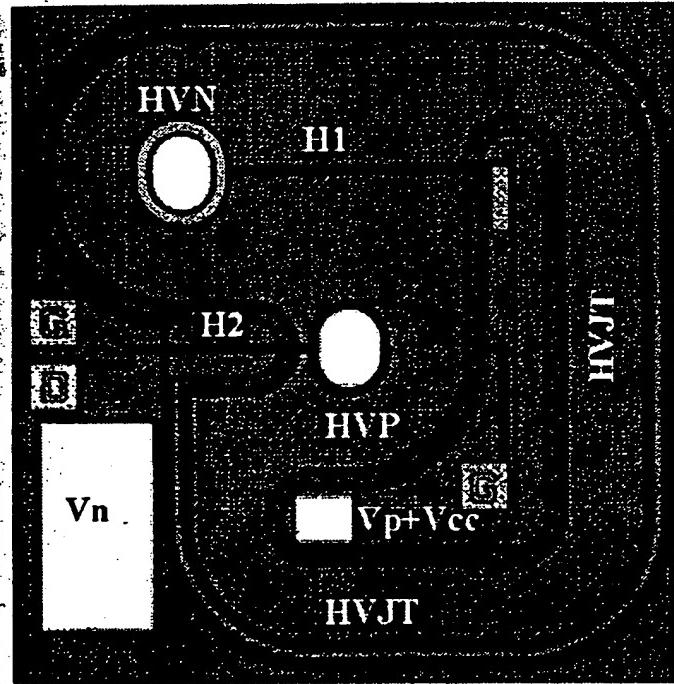
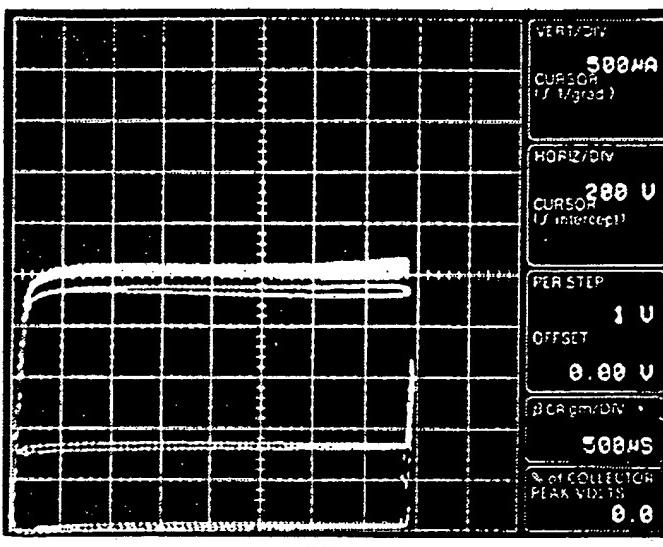
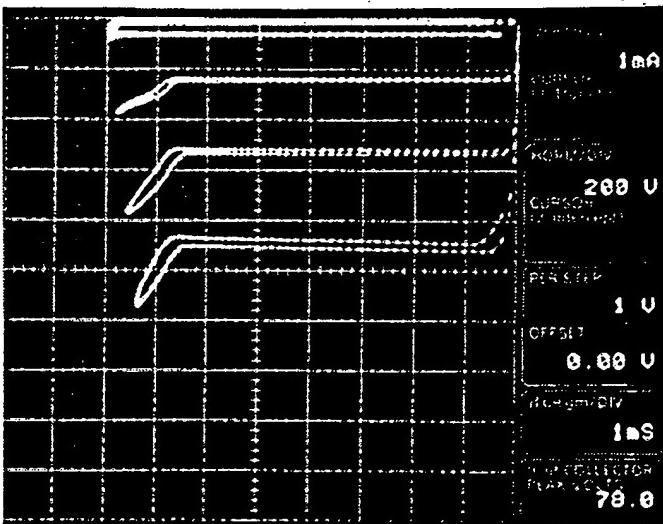


Fig. 4 Photograph of the experimental, complementary, self-shielded, high-voltage level-shifters in a single device layout.

The output characteristics of HVN and HVP are shown in Fig. 5 (a) and (b), respectively. Both HVN and HVP have a breakdown voltage of 1600V. As the doping of diffused regions were not optimized, the threshold voltage of HVN was much lower than that of HVP. The kink of output characteristics of HVP at high-current and high-voltage region is also due to the same reason. In HVN, the saturation of output current independent of gate voltage at higher gate



(a)



(b)

Fig. 5 Output characteristics of (a) HVN and (b) HVP.

voltage region comes from the effect of its double-base structure.

The operations of self-shielded, high-voltage, complementary level-shifters under 1200V supply are shown in Fig. 6 (a) and (b). The n-channel level-shifter converted the V_n -level, 0V/2V input signal to V_o -level, 1200V/1120V output signal. The p-channel level-shifter converted the V_o -level, 1200V/1185V input signal to V_n -level, 0V/40V signal. From these operation wave-forms, it is confirmed that the self-shielded level-shifters fulfill their function excellently in very high-voltage ICs.

For evaluating parasitic resistors, R_{p1} and R_{p2} , leakage currents, I_{rp1} and I_{rp2} , respectively through R_{p1} and R_{p2} , were measured. They are plotted in Fig. 7 as a function of